



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,827	01/03/2001	Ashok Krishnamurthi	0023-0027	9945

44987 7590 07/29/2004

HARRITY & SNYDER, LLP  
11240 WAPLES MILL ROAD  
SUITE 300  
FAIRFAX, VA 22030

EXAMINER

LEE, ANDREW CHUNG CHEUN

ART UNIT PAPER NUMBER

2664

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/752,827

Applicant(s)

KRISHNAMURTHI ET AL.

Examiner

Andrew C Lee

Art Unit

2664

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-17,20,22-25,27 and 28 is/are rejected.
- 7) ☒ Claim(s) 18 and 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 7-23-02.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Fig. 3 Frame Deframer Module 330. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Specification***

2. The disclosure is objected to because of the following informalities:
- Page 6, line 17, the Office suggests the element “framer module 330” should be corrected as “Framer Deframer module 330” so as in consistent with Fig. 3 claimed. The correct element should be “Framer/Deframer Module 330”.
  - Page 7, lines 18, 20, 21, the Office suggests the element “framer module 330” should be corrected as “Framer Deframer module 330” so as in consistent with Fig. 3 claimed.
  - Page 8, lines 1,5, 6, 8, 12, 13, 14, 20-21, the Office suggests the element “framer module 330” should be corrected as “Framer Deframer module 330” so as in consistent with Fig. 3 claimed.

Art Unit: 2664

- Page 9, lines 7, 22, the Office suggests the element “framer module 330” should be corrected as “Framer Deframer module 330” so as in consistent with Fig. 3 claimed.

Appropriate correction is required.

### ***Claim Objections***

3. Claims 18 and 19 are objected to because of the following informalities:
    - Pag18, line 1, the Office requests the clarification from the applicant for the term “a first clock rate” disclosed in claim 18 (a framer module, operating at a first clock rate). Is this “first clock rate” same as the “first clock rate” disclosed in claim 1.
    - Pag18, line 6, the Office requests the clarification from the applicant for the term “a second clock rate” disclosed in claim 19 (a receiver module, operating at a second clock rate). Is this “second clock rate” same as the “first clock rate” disclosed in claim 1.
- . Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
5. Claims 18 and 19 recite the limitation “a framer module, operating at a first clock rate” in Page 18 , Line 1, and “ a receiver module, operating at a second

Art Unit: 2664

clock rate" in page 18, Line 6. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-2, 4-19, 20, 22-25, 27-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Theodoras et al (US Pat. No. 6751743 B1).

Regarding claim 1, Theodoras et al discloses the limitation of an apparatus for interfacing a high-speed link to a network device, comprising a receiver module, operating at a first clock rate, for receiving a stream of incoming data from the high-speed link (*Fig. 6, column 8, lines 51-53*); a framer module, operating at a second clock rate, for deserializing the stream of incoming data onto a multi-line bus and extracting data packets from the deserialized data on the multi-line bus (*Fig. 6, column 6, lines 54-55*), wherein the second clock rate is lower than the first clock rate (*column 8, lines 56-58*).

Art Unit: 2664

Regarding claims 2 and 20, Theodoras et al discloses the limitation of the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-192 link (*Fig. 6, column 8, lines 52-53*).

Regarding claim 4, Theodoras et al discloses the limitation of receiving the extracted data packets from the framer module and transmitting each extracted data packet to one of a plurality of processing paths in the network device (*column 8, lines 54-58*).

Regarding claim 5, Theodoras et al discloses the apparatus comprising a sprayer module for receiving the extracted data packets from the framer module and transmitting each extracted data packet to one of a plurality of witching/forwarding module for processing (*column 8, lines 54-58; column 5, lines 51-54*).

Regarding claim 6, Theodoras et al discloses the apparatus comprising a plurality of preprocessing modules for processing data packets (*Fig 5, column 7, lines 23-29*); and a sprayer module for receiving the extracted data packets from the framer module (*Fig. 6, column 8, lines 50-56*) and transmitting each extracted data packet to one of the plurality of preprocessing modules (*column 8, lines 55-58*).

Regarding claim 7, Theodoras et al discloses the limitation of the apparatus comprising a plurality of memories, each memory corresponding to

Art Unit: 2664

one of the plurality of preprocessing modules (*Fig. 5, column 7, lines 23-26; column 8, lines 28-30*) and each preprocessing module comprises a memory management module for storing portions of data packets into its corresponding memory (*column 8, lines 23-28*).

Regarding claim 8, Theodoras et al discloses the limitation of apparatus comprising the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, and the plurality of memories are mounted onto a single board (*column 9, lines 2-7*).

Regarding claim 9, Theodoras et al discloses the limitation of the apparatus comprising the receiver module, the framer module, the sprayer module, the plurality of preprocessing modules, and the plurality of memories are integrated onto a single chip (*column 9, lines 2-7*).

Regarding claim 10, Theodoras et al discloses the limitation of the apparatus comprising: a deframer module, operating at the second clock rate, for receiving data packets and processing the data packets into a stream of outgoing data for transmission on the high-speed link (*Fig. 6, column 8, lines 59-64*); a transmitter module, operating at the first clock rate, for transmitting the stream of out-going data onto the high-speed link (*Fig. 6, column 8, line 67, column 9, lines 1-2*).

Art Unit: 2664

Regarding claim 11, Theodoras et al discloses the apparatus comprising: a desprayer module for receiving data packets from a plurality of processing paths and transmitting the received data packets to the deframer module (*Fig. 6, column 8, lines 59-65*).

Regarding claim 12, Theodoras et al discloses the limitation of an apparatus for interfacing at least one line interface card to a plurality of switching/forwarding modules of a network device (*Fig. 4*), comprising a plurality of preprocessing modules for processing data packets and transmitting the processed data packets to respective switching/forwarding modules (*Fig. 4, column 5, lines 52-59*); a sprayer module for receiving data packets from at least one line interface card and transmitting each received data to one of the plurality of preprocessing modules (*column 6, lines 19-26*).

Regarding claim 13, Theodoras et al discloses the limitation of the apparatus comprising a plurality of memories, each memory corresponding to one of the plurality of preprocessing modules (*Fig. 5, column 7, lines 23-26; column 8, lines 28-30*) and each preprocessing module comprises a memory management module for storing portions of data packets into its corresponding memory (*column 8, lines 23-28*).

Regarding claim 14, Theodoras et al teaches the limitation of the plurality of preprocessing modules, the plurality of memories, and the sprayer modules



Art Unit: 2664

are mounted onto a single board (*column 7, lines 65-76, column 8, lines 1-4; column 9, lines 2-7*).

Regarding claim 15, Theodoras et al also teaches the limitation of the plurality of preprocessing modules, the plurality of memories, and the sprayer modules are integrated onto a single chip (*Fig 6, column 8, lines 50-51*).

Regarding claim 16, Theodoras et al discloses the limitation of the apparatus comprising: a desprayer module for receiving data packets from the plurality of preprocessing modules (*Fig. 5, lines 14-19*) and outputting the received data packets to the line interface card (*Fig. 5, lines 14-15*).

Regarding claim 17, Theodoras et al discloses the limitation of a networking device comprising a sprayer module for receiving data packets and outputting the received data packets on a plurality of channels (*Fig. 4, column 5, lines 52-56*); a plurality of preprocessing modules for processing data packets, each preprocessing module receiving data packets from one of the channels of the sprayer module (*Fig. 4, lines column 6, lines 19-22*); and a plurality of switching/forwarding modules, each switching/forwarding module receiving data packets from a corresponding one of the plurality of preprocessing modules (*Fig. 4, column 6, lines 23-29*).

Regarding claim 18, Theodoras et al discloses a framer module operating at a first clock rate, for deserializing the stream of in-coming data onto a multi-line bus and extracting data packets from the deserialized data on the multi-line bus

Art Unit: 2664

and transmitting the extracted data packets to the sprayer module(*Fig. 6, column 6, lines 54-55*).

Regarding claim 19, Theodoras et al discloses the limitation of a network device comprising a receiver module, operating at a second clock rate, for receiving a stream of in-coming data from a high-speed link and transmitting of in-coming data to the framer module (*Fig. 6, column 8, lines 51-53*); wherein the first clock rate is lower than the second clock rate.

Regarding claim 22, Theodoras et al discloses networking device comprising: a desprayer module for receiving data packets on a plurality of channels (*Fig 4, column 5, lines 56-59*) each corresponding to one of the plurality of preprocessing modules (*Fig 4, column 5, lines 58-59*).

Regarding claim 23, Theodoras et al discloses the limitation of the networking device comprising: a deframer module, operating at a first clock rate (*Fig 6, column 8, lines 59-60*), for receiving data packets from the desprayer module and processing the data packets into a stream of out-going data for transmission on a high-speed link (*column 8, lines 59-62*).

Regarding claim 24, Theodoras et al discloses the limitation of the networking device comprising a transmitter module, operating at a second clock rate (*Fig. 6, column 8, lines 59-60*) for transmitting the stream of out-going data

Art Unit: 2664

onto the high-speed link (*column 8, lines 61-62*), wherein the first clock rate is lower than the second clock rate (*column 8, lines 59-62*).

Regarding claim 25, Theodoras et al teaches the limitation of the transmitter module comprises optics and circuitry for transmitting optical signals onto a SONET OC-192 link (*column 8, lines 61-63*).

Regarding claim 27, Theodoras et al discloses the limitation of receiving data from a high-speed link (*Fig 6*), comprising receiving a stream of data signals at a data rate of at least approximately 10 Gigabits per second (*column 8, lines 51-54*); deserializing the stream of data signals onto a multi-line bus (*column 8, lines 54-55*); extracting data packets from the deserialized data (*column 8, lines 55-56*); spraying the data packets across a plurality of processing paths (*column 8, lines 56-58*).

Regarding claim 28, Theodoras et al discloses the limitation of receiving data to a high-speed link (*Fig. 6*), comprising of receiving data packets from a plurality of processing paths (*column 8, lines 59-60*); processing the data packets for transmission on the high-speed link (*column 8, lines 60-61*); serializing the processed data packets to form a stream of data signals (*column 8, lines 61-62*); transmitting the stream of data signals to the high-speed link (*column 8, lines 61-63*).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3, 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Theodoras et al (US Pat. No. 6751743 B1) in view of Patwardhan et al (US Pat. No. 6741615 B1).

Regarding claims 3 and 21, Theodoras et al discloses the limitation of the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-192 link (*Fig. 6, column 8, lines 52-53*). He does not disclose the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-768. Patwardhan et al discloses the receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-768 (*column 8, lines 23-27*). Therefore, it would have been obvious to modify Theodoras et al in include a receiver module comprising optics and circuitry for receiving optical signals from a SONET OC-768 as that taught by Patwardhan et al in order to have high speed SONET connection and network throughput.

Regarding claim 26, Theodoras et al discloses the limitation of the receiver module comprising optics and circuitry for transmitting optical signals

Art Unit: 2664

from a SONET OC-192 link (*Fig. 6, column 8, lines 61-62*). He does not disclose the receiver module comprising optics and circuitry for transmitting optical signals from a SONET OC-768. Patwardhan et al discloses the transmitter module comprising optics and circuitry for transmitting optical signals from a SONET OC-768 (column 8, lines 23-27). Therefore, it would have been obvious to modify Theodoras et al in include a transmitter module comprising optics and circuitry for transmitting optical signals from a SONET OC-768 as that taught by Patwardhan et al in order to have high speed SONET connection and network throughput.

### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew C Lee whose telephone number is (703) 305-8086. The examiner can normally be reached on Monday through Friday from 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (703) 305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2664

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ACL 12 July 2004

  
Ajit Patel  
Primary Examiner